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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/532,456	GUNTER ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-10,12-14 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-10,12-14 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

The indicated allowability of claims 2-8 and 11 is withdrawn in view of the newly discovered reference(s) to Khan et al (US Patent 6,690,042) and Cachier et al, US Patent 5,715,897. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 3, 6, 8, 12, 14, 22-24, and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Regarding claims 3, 6, 12, 14, 24 and 26, the term "about" is a relative term, which renders the claim indefinite. The term "term" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Examiner is unsure as to what specific value or range of values would be

acceptable in the use of the term "about" (for example, in claim 26, which recites that the collector finger width is "about 2 μm", would collector finger widths of 3 μm, 1μm or 15 μm meet this limitation?).

4. Regarding claim 8, the limitation "anneal is performed post-bake metallization" is recited in the 2nd line of this claim. There is insufficient antecedent basis for this limitation in the claim because claim 22, on which claim 8 is dependent, has failed to mention a post-bake metallization. Examiner is unsure if the anneal is the post-bake process of if there is a post-bake process, then the annealing.

5. Regarding claim 22, the phrase "directionally etching to remove silicon nitride on planes parallel to the n+ GaN quasi-substrate layer" in claim 22 is a relative phrase which renders the claim indefinite. The phrase " directionally etching to remove silicon nitride on planes parallel to the n+ GaN quasi-substrate layer " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is unclear as to what direction the etching is to take place on the silicon nitride layer. While the claim states the directional etching to remove the silicon nitride occurs on planes parallel to the n+ GaN layer, it is unclear as to which n+GaN plane the claims are referring.

6. Regarding claim 23, the limitation "the emitter ohmic metallization layer" is recited in first line of the claim. There is insufficient antecedent basis for this limitation in the claim because claim 22, on which claim 23 is dependent, has failed to mention the ohmic metallization layer is for the emitter.

7. Claims 1 and 22 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

The omitted steps are the forming the n- GaN layer and the steps that explain which n^+ GaN layer is being referred for the following limitations" "opening an window for collector fingers using E-beam lithography", "depositing an ohmic metallization layer over the window for the collector fingers", "lifting-off ohmic metallization, thereby forming the collector fingers", "opening a window for a self-aligned base recess using optical lithography", opening a window for a collector contact pad, using optical lithography", "depositing a high quality silicon nitride layer over the window for a collector contact pad", and "lifting-off or wet chemical etching the high quality silicon nitride layer, thereby forming a silicon nitride collector contact pad".

Claim Objections

1. Claims 1 and 22 are objected to because of the following informalities. Appropriate correction is required.

2. Claims 1 and 22 recite a limitation of "etching to recess a base layer to an n-GaN quasi-substate layer grown on the n^+ GaN quasi substrate layer". However, prior to this recitation, there has not been a recitation of the existence of an n^- GaN layer on the n^+ GaN quasi-substrate.

3. Claims 1 and 22 recite a limitation concerning the formation of ohmic metallization layer, which has caused some confusion as to which semiconductor layer this metallization is being fabricated upon. From the claim language, one may deduce that the ohmic metallization is being performed for the formation of the collector contact layer, as shown in figure 1B.

However, it is unclear as to which semiconductor layer this ohmic metallization is being conducted to or upon. While figure 1b shows a collect contact layer formed on a second n^+ GaN layer, this second n^+ GaN layer is not the same as the first n^+ GaN layer that has been referred to earlier in the claim because the second n^+ GaN layer is grown by molecular beam epitaxy (MBE) instead of HVPE, which is how the first n^+ GaN layer was grown (see Applicant's Specification, paragraph 8). Examiner is requesting the

clarification as to which n^+ GaN layer is being referred to for each of the processing steps.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-6, 9, 10, and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaudo et al, US Patent 6,156,581 in view of Kawai et al, US Patent 5,929,467, Romankiw, US Patent 4,224,361, Parikh et al, US Patent Application 2003/0015708, Cheng et al, US Patent 5,215,619, Khan et al, US Patent 6,690,042 and Cachier et al, US Patent 5,175,597.

3. Regarding claim 1, Vaudo teaches a method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising of a hydride vapor phase epitaxy (HVPE) grown n+ GaN quasi-substrate (column 6, lines 50-51, column 12, lines 51-60) and forming collector fingers **192**.

Vaudo fails to teach opening a window for helium implantation on a GaN layer, using optical lithography, implanting helium on the GaN layer over the window for helium implantation, so as to provide an insulating layer for contact pads of the device, opening a window for collector fingers using E-beam lithography, depositing an ohmic metallization layer over the window for the collector fingers, lifting-off ohmic metallization to form the collector fingers, opening a window for a self-aligned base recess using optical lithography, and etching to recess a base layer to an n- GaN layer grown on the n+ GaN layer, wherein the etching is performed with a ramp down in chuck bias voltage, opening a window for a collector contact pad, using optical lithography depositing a high quality silicon nitride layer over the window for a collector contact pad, and lifting off or wet etching the high quality silicon nitride layer, thereby forming a silicon nitride collector contact pad.

Kawai teaches opening a window for helium implantation on a GaN layer, using optical lithography (column 4, lines 10-15 and column 5, lines 33-36) and implanting helium on the GaN layer over the window for helium implantation, so as to provide an insulating layer for contact pads **17** (figure 5) of the device (column 5, lines 33-36 figure 8) because in addition to the ability to form an insulating layer for a contact pad, selective implantation of helium into a substrate is performed as a method for formation of insulating separating portion, which can also serve to separate the FET from other devices.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kawai with that of Vaudo because in addition to the ability to form an insulating layer for a contact pad, selective implantation of helium into a substrate is performed as a method for formation of insulating separating portion, which can also serve to separate the FET from other devices.

Vaudo and Kawai fail to teach opening a window for collector fingers using E-beam lithography, depositing an ohmic metallization layer over the window for the collector fingers, and lifting-off ohmic metallization to form the collector fingers, opening a window for a self-aligned base recess using optical lithography; and etching to recess a base layer to an n- GaN quasi-substrate layer grown on the n+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage, opening a window for a collector contact pad, depositing a high quality silicon nitride layer over the window for a collector contact pad, and lifting off or wet etching the high quality silicon nitride layer, thereby forming a silicon nitride collector contact pad.

Romankiw teaches opening a window **50** for collector fingers using E-beam lithography **52,** depositing an ohmic metallization layer **25** over the window for the collector fingers, and lifting-off ohmic metallization to form the collector fingers (figures 3a-3c and column 5, lines 22-30) as a simple, conventionally-known technique that is used to deposit metallic layers onto a substrate.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Romankiw with that of Vaudo and Kawai as a simple, conventionally known technique that is used to deposit metallic layers onto a substrate.

Vaudo, Kawai, and Romankiw fail to teach opening a window for a self-aligned base recess using optical lithography; and etching to recess a base layer to an n- GaN quasi-substrate layer grown on the n+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage, opening a window for a collector contact pad, depositing a high quality silicon nitride layer over the window for a collector contact pad, and lifting off or wet etching the high quality silicon nitride layer, thereby forming a silicon nitride collector contact pad.

Parikh teaches opening a window for a self-aligned base recess using optical lithography and etching to recess a base layer to an n- GaN quasi-substrate layer **52** grown on the n+ GaN quasi-substrate layer **53** ([0049, 0004-0013] Note: Parikh teaches the use of a dry etch, RIE, to etch the base layer. It is well-known in the art that RIE etching uses a photoresist with an opening window that is used to designate in which areas the etching process is to take place) as a method of forming a GaN base layer, which provides for a low on-state voltage, a desirable trait for diodes, without increasing the reverse leakage current, an undesirable trait.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Parikh with that of Vaudo, Kawai, and Romankiw as a method of forming a GaN base layer, which provides for a low on-state voltage, a desirable trait for diodes, without increasing the reverse leakage current, an undesirable trait.

Vaudo, Kawai, Romankiw, and Parikh fails to teach the etching is performed with a ramp down in chuck bias voltage, opening a window for a collector contact pad, depositing a high quality silicon nitride layer over the window for a collector contact pad, and lifting off or wet etching the high quality silicon nitride layer, thereby forming a silicon nitride collector contact pad.

Cheng teaches the etching is performed with a ramp down in chuck bias voltage (column 10, lines 5-12) when the magnetic field in the etching chamber is increased, which reduces the ion bombardment of the wafer and reduces device damage.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Cheng with that of Vaudo, Kawai, Romankiw, and Parikh because decreasing the RF power and subsequent bias voltage reduces the ion bombardment of the wafer and reduces device damage.

Vaudo, Kawai, Romankiw, Parikh, and Cheung fail to teach opening a window for a collector contact pad, depositing a high quality silicon nitride layer over the window for

a collector contact pad, and lifting off or wet etching the high quality silicon nitride layer, thereby forming a silicon nitride collector contact pad.

Khan teaches teach opening a window for a collector contact pad, depositing a high quality silicon layer **36** over the window for a collector contact pad, and lifting off or wet etching the high quality silicon layer, thereby forming a silicon collector contact pad (column 3, lines 35-40, column 4, lines 34-55) as a layer that provides high quality passivation and significantly reduces the reverse leakage.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Khan with that of Vaudo, Kawai, Romankiw, Parikh, and Cheung because a silicon passivation layer between the ohmic contact and the semiconductor substrate provides high quality passivation and significantly reduces the reverse leakage.

Vaudo, Kawai, Romankiw, Parikh, Cheung, and Khan fail to teach the silicon layer is a silicon nitride layer.

Cachier teaches a silicon layer is a silicon nitride layer (column 9, line 64 to column 10, lines 5) as a layer to passivate the exposed channels and sides of the permeable-based transistor. Silicon nitride is the preferred passivation layer because it

does not allow contaminants such as sodium ions to penetrate the layer, unlike silicon dioxide.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cachier with that of Vaudo, Kawai, Romankiw, Parikh, Cheng, and Khan because silicon nitride is the preferred passivation layer because it does not allow contaminants such as sodium ions to penetrate the layer, unlike silicon dioxide.

4. Regarding claim 3, Khan teaches the silicon nitride layer is deposited over the window for helium implantation via plasma enhanced chemical vapor deposition (column 4, lines 45-49. Note, while Khan does not teach a silicon nitride layer, Cachier teaches that a silicon nitride passivation layer that may be substituted for silicon dioxide since silicon nitride is a better passivation layer).

Vaudo, Kawai, Romankiw, Parikh, Cheung, Khan and Cachier fail to the silicon nitride layer is about 1000-2000 Angstroms thick.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected

result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

5. Regarding claim 4, Khan teaches opening a window for Ti metallization of the collector contact pad using optical lithography and depositing Ti over the window for Ti metallization of the collector contact pad, thereby forming a Ti collector contact pad (column 51-56).

Khan fails to teach a lift-off process.

Romankiw teaches the use of a lift-off process (figures 3a-3c and column 5, lines 22-30) as a simple, conventionally known technique that is used to deposit metallic layers onto a substrate.

6. Regarding claim 5, Khan teaches opening a window for a second Ti metallization of the collector contact pad using optical lithography, depositing Ti over the window for

the second Ti metallization of the collector contact pad, thereby forming a Ti cap over the collector contact pad.

Khan fails to teach a lift-off process.

Romankiw teaches the use of a lift-off process (figures 3a-3c and column 5, lines 22-30) as a simple, conventionally known technique that is used to deposit metallic layers onto a substrate.

7. Regarding claim 6, Khan teaches depositing Ti over the window for Ti metallization of the collector contact pad includes depositing Ti/Au using E-beam evaporation (column 4, lines 50-56).

Vaudo, Kawai, Romankiw, Parikh, Cheung, Khan and Cachier fail to teach depositing Ti/Au at thicknesses of about 500 Angstroms/ 1000 Angstroms, respectively.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere

dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

8. Regarding claim 9, Parikh further teaches opening an emitter etch/contact window using optical lithography [0049] and the n+ GaN quasi-substrate layer.

Parikh fail to teach etching an emitter recess to the quasi-substrate layer, depositing an emitter ohmic metallization layer over the etched emitter recess, and lifting-off emitter ohmic metallization, thereby forming an emitter contact pad.

However, Romankiw further teaches etching an emitter recess to the quasi-substrate layer, depositing an emitter ohmic metallization layer over the etched emitter recess, and lifting-off emitter ohmic metallization, thereby forming an emitter contact pad (figures 3a-3c and column 5, lines 22-30).

9. Regarding claim 10, Kawai further teaches the emitter ohmic metallization layer includes at least one of titanium, aluminum, nickel, and gold (column 4, lines 5-9).

10. Regarding claim 12, Vaudo, Kawai, Romankiw, Parikh, Cheung, Khan and Cachier fail to teach the helium implantation is achieved with an implant depth of about 2 μm.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

11. Regarding claim 13, Romankiw further teaches the ohmic metallization layer over the window for the collector fingers is Ti/Ni (column 1, lines 60-67).

Vaudo, Kawai, Romankiw, Parikh, Cheung, Khan and Cachier fail to teach the collector fingers with thicknesses of 100A and 400A, respectively.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

12. Regarding claim 14, Vaudo further teaches the device has a plurality of collector fingers having a finger pitch between1: 1 and 1:3 (evenly spaced. See figure 15).

Vaudo, Kawai, Romankiw, Parikh, Cheung, Khan and Cachier fail to teach the collector fingers about 0.2 μm wide.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed

that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

13. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parikh et al, US Patent Application 2003/0015708 in view of Cheng et al, US Patent 5,215,619 and Previti-Kelly, US Patent 5,006,488.

14. Regarding claim 21, Parikh teaches a method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising of opening a window for a base recess, opening a window for RF test pad metallization using optical lithography, depositing RF test pad metallization layer, thereby providing RF test pads **55a** ([0049] Note: Parikh teaches the use of a dry etch, RIE, to etch the base layer. It is well-known in the art that RIE etching uses a photoresist with an opening window that is used to designate in which areas the etching process is to take place); and etching to recess a base layer to an n- GaN quasi-substrate layer **53** grown on the n+ GaN quasi-

substrate layer **52**. In addition, Parikh teaches the formation of ohmic metal contacts **55a, 55b.** These contacts could then be connected to a test pads and connected to a testing apparatus to determine if the transistor works by sending RF power to the transistor).

Parikh fails to teach the etching is performed with a ramp down in chuck bias voltage and forming the test pad metallization by a lift-off process.

However, Cheng teaches the etching is performed with a ramp down in chuck bias voltage (column 10, lines 5-12) when the magnetic field in the etching chamber is increased, which reduces the ion bombardment of the wafer and reduces device damage.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Cheng with that of Parikh because decreasing the RF power and subsequent bias voltage reduces the ion bombardment of the wafer and reduces device damage.

Parikh and Chang fail to teach forming the test pad metallization by a lift-off process.

Previti-Kelly teaches forming the test pad metallization by a lift-off process (figures 1-4) as a commonly employed method for better selectivity deposition for metallic deposition.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Previti-Kelly with that of Parikh and Chang because a lift-off technique is a commonly employed method for better selectivity deposition for metallic deposition.

15. Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaudo et al, US Patent 6,156,581 in view of Kawai et al, US Patent 5,929,467, Romankiw, US Patent 4,224,361, Parikh et al, US Patent Application 2003/0015708, Cheng et al, US Patent 5,215,619, and Cachier et al, US Patent 5,175,597.

16. Regarding claim 22, Vaudo teaches a method for fabricating an etched grooved GaN-based permeable-base transistor device, comprising of a hydride vapor phase epitaxy (HVPE) grown n+ GaN quasi-substrate (column 6, lines 50-51, column 12, lines 51-60) and forming collector fingers **188**, and depositing a base metallization layer, thereby forming a base contact pad **196**.

Vaudo fails to teach opening a window for helium implantation on a GaN layer, using optical lithography, implanting helium on the GaN layer over the window for

helium implantation, so as to provide an insulating layer for contact pads of the device, opening a window for collector fingers using E-beam lithography, depositing an ohmic metallization layer over the window for the collector fingers, lifting-off ohmic metallization to form the collector fingers, opening a window for a self-aligned base recess using optical lithography, etching to recess a base layer to an n- GaN layer grown on the n+ GaN layer, wherein the etching is performed with a ramp down in chuck bias voltage, depositing a conformal silicon nitride for passivation of the recessed base layer, directionally etching to remove the silicon nitride layer on planes parallel to the n+ GaN quasi-substrate layer, and forming the base contact by a lift-off process.

Kawai teaches opening a window for helium implantation on a GaN layer, using optical lithography (column 4, lines 10-15 and column 5, lines 33-36) and implanting helium on the GaN layer over the window for helium implantation, so as to provide an insulating layer for contact pads **17** (figure 5) of the device (column 5, lines 33-36 figure 8) because in addition to the ability to form an insulating layer for a contact pad, selective implantation of helium into a substrate is performed as a method for formation of insulating separating portion, which can also serve to separate the FET from other devices.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kawai with that of Vaudo because in addition to the ability to form an insulating layer for a contact pad, selective implantation of helium into a

substrate is performed as a method for formation of insulating separating portion, which can also serve to separate the FET from other devices.

Vaudo and Kawai fail to teach opening a window for collector fingers using E-beam lithography, depositing an ohmic metallization layer over the window for the collector fingers, and lifting-off ohmic metallization to form the collector fingers, opening a window for a self-aligned base recess using optical lithography, etching to recess a base layer to an n- GaN quasi-substrate layer grown on the n+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage, depositing a conformal silicon nitride for passivation of the recessed base layer, directionally etching to remove the silicon nitride layer on planes parallel to the n+ GaN quasi-substrate layer, and forming the base contact by a lift-off process.

Romankiw teaches opening a window **50** for collector fingers using E-beam lithography **52,** depositing an ohmic metallization layer **25** over the window for the collector fingers, and lifting-off ohmic metallization to form the collector fingers forming the base contact by a lift-off process (figures 3a-3c and column 5, lines 22-30) as a simple, conventionally-known technique that is used to deposit metallic layers onto a substrate.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Romankiw with that of Vaudo and Kawai as a simple, conventionally known technique that is used to deposit metallic layers onto a substrate.

Vaudo, Kawai, and Romankiw fail to teach opening a window for a self-aligned base recess using optical lithography, etching to recess a base layer to an n- GaN quasi-substrate layer grown on the n+ GaN quasi-substrate layer, wherein the etching is performed with a ramp down in chuck bias voltage, depositing a conformal silicon nitride for passivation of the recessed base layer, directionally etching to remove the silicon nitride layer on planes parallel to the n+ GaN quasi-substrate layer.

Parikh teaches opening a window for a self-aligned base recess using optical lithography and etching to recess a base layer to an n- GaN quasi-substrate layer **52** grown on the n+ GaN quasi-substrate layer **53** ([0049, 0004-0013] Note: Parikh teaches the use of a dry etch, RIE, to etch the base layer. It is well-known in the art that RIE etching uses a photoresist with an opening window that is used to designate in which areas the etching process is to take place) as a method of forming a GaN base layer, which provides for a low on-state voltage, a desirable trait for diodes, without increasing the reverse leakage current, an undesirable trait.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Parikh with that of Vaudo, Kawai, and Romankiw as a method

of forming a GaN base layer, which provides for a low on-state voltage, a desirable trait for diodes, without increasing the reverse leakage current, an undesirable trait.

Vaudo, Kawai, Romankiw, and Parikh fail to teach the etching is performed with a ramp down in chuck bias voltage, depositing a conformal silicon nitride for passivation of the recessed base layer, directionally etching to remove the silicon nitride layer on planes parallel to the n+ GaN quasi-substrate layer.

Cheng teaches the etching is performed with a ramp down in chuck bias voltage (column 10, lines 5-12) when the magnetic field in the etching chamber is increased, which reduces the ion bombardment of the wafer and reduces device damage.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Cheng with that of Vaudo, Kawai, Romankiw, and Parikh because decreasing the RF power and subsequent bias voltage reduces the ion bombardment of the wafer and reduces device damage.

Vaudo, Kawai, Romankiw, Parikh, and Cheng fail to teach depositing a conformal silicon nitride for passivation of the recessed base layer, directionally etching to remove the silicon nitride layer on planes parallel to the n+ GaN quasi-substrate layer.

Cachier teaches depositing a conformal silicon nitride **23** for passivation of the recessed base layer and directionally etching to remove the silicon nitride layer on planes parallel to the n+ GaN quasi-substrate layer (column 9, line 64 to column 10, lines 5) to passivate the exposed channels and sides of the permeable-based transistor. Silicon nitride is the preferred passivation layer because it does not allow contaminants such as sodium ions to penetrate the layer, unlike silicon dioxide.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Cachier with that of Vaudo, Kawai, Romankiw, Parikh, and Cheng because silicon nitride is the preferred passivation layer because it does not allow contaminants such as sodium ions to penetrate the layer, unlike silicon dioxide.

17. Regarding claim 23, Vaudo teaches the emitter ohmic metallization layer includes at least one of titanium, aluminum, nickel, and gold (column 18, line 33).

18. Regarding claim 24, Vaudo, Kawai, Romankiw, Parikh, Cheng, and Cachier fail to teach the helium implantation is achieved with an implant depth of about 2 μm.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed

that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

19. Regarding claim 25, Vaudo, Kawai, Romankiw, Parikh, Cheng, and Cachier fail to teach the ohmic metallization over the window for the collector finger us Ti/Ni with a thickness of 100 Angstroms and 400 Angstroms, respectively.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise

critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

20. Regarding claim 26, Vaudo further teaches the device has a plurality of collector fingers having a finger pitch between1: 1 and 1:3 (evenly spaced. See figure 15).

Vaudo, Kawai, Romankiw, Parikh, Cheng, and Cachier fail to teach the device has a plurality of collector fingers about 0.2 μm wide.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc.,

725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

21. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vaudo, Kawai, Romankiw, Parikh, Cheng, and Cachier as applied to claim 22 above, and further in view of Bhatnagar et al, US Patent 5,895,260.

22. Regarding claim 8, Vaudo, Kawai, Romankiw, Parikh, Cheng, and Cachier fail to teach an anneal is performed post-bake metallization so as to provide the base contact pad with low reverse current leakage and low contact resistance.

Bhatnagar teaches an anneal is performed post-bake metallization so as to provide the base contact pad with low reverse current leakage and low contact resistance (with the anneal being the post bake metallization process, column 3, lines 62-67) as part of the process used in order to form an ohmic contact with the substrate

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Bhatnagar with that of Vaudo, Kawai, Romankiw, Parikh, Cheng, and Cachier because annealing is conducted during semiconductor formation because high temperature annealing may recrystallize the damage structure in areas to the point that they would no longer be highly resistive.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-6, 8-14, and 21-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent Application Publication 2003/0151046, issued to Brar et al; US Patent 5,571,732, issued to Liu; US Patent 5,270,554, issued to Palmour; US Patent 4,510,016, issued to Chi et al; US Patent Application Publication 2002/0190273; and Calviello, US Patent 4,701,996.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 7AM to 3:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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QVJ

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